Alpha Language Semantics

Assignment

New VAR

<register var>

New VAR = LITERAL:

<register var>

“load <var\_reg> LITERAL”

Const var = LITERAL:

<register const>

Delete VAR:

<deregister var>

VAR = CONST:

“loadi <var\_reg> {addr of const}”

LVAR = RVAR:

“andi reg[LVAR] 0”

“add reg[LVAR] reg[RVAR]”

“ASSEMBLY STATEMENT”:

asmCode.push\_back(ASSEMBLY\_STATEMENT)

pseudo code

int stack[initial\_size]

int assemblyCode[initial\_size]

line = readline()

for each c in line:

if “CONST”